REMARKS

Claims 1-34 are currently pending in the application. The Examiner rejected claims 1-12, 14, 15, 17-23, 27-31, 33 and 34. The Examiner objected to claims 13, 16, 24-26 and 32.

The Examiner objected to the specification as missing page 26. A copy of originally filed page 26 has been submitted herewith in the attached Appendix and the objection is believed addressed thereby. A copy of the stamped receipt post card indicating receipt by the Patent Office of all pages of the applications has also been provided. No new matter is introduced.

The Examiner reiterated here rejection of claims 1-6, 9, 11, 14, 15, 17-23, 27, 28, 30, 33 and 34 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication 2002/0023255 (Karniewicz). The rejection is respectfully traversed.

Karniewicz describes a hierarchical semiconductor design which includes several levels of abstraction (Abstract). In referring to Figs. 1(a)-1(c), Karniewicz describes four levels of a hierarchical semiconductor test structure. Fig. 1(a) shows two levels of the hierarchy, one being the so-called "higher level cells" 100, 110 and 112, and the other being the lowest level of the hierarchy, so-called "basic atom cells" 102-108 in higher level cell 100, 114-118 in higher level cell 110, and 120-130 in higher level cell 112. See paragraphs [0026]-[0028].

Fig. 1(b) introduces another level to the hierarchy, referred to as the "device" level, which includes devices 132 and 140. Device 132 includes three higher order cells 134-138, and device 140 includes two higher order cells 142 and 144. Finally Fig. 1(c) introduces the fourth and highest level of the hierarchy, the semiconductor test structure 146 which includes three devices 148-152. See paragraphs [0030]-[0035].

While Karniewicz does refer to the changing of parameters (e.g., size and placement) associated with various cells in the hierarchy, it does so merely to make the point that such changes are propagated to affected cells on other levels of the hierarchy (e.g., see paragraphs [0027] and [0031]).

Karniewicz does not, however, teach the sizing of transistors for each of a plurality of cell instances such that each cell type is divided into a plurality of subtypes. Neither does it teach the merging of selected subtypes such that the number of subtypes for at least one cell type is reduced. Finally, it does not teach such a merging step as achieving "a balance between the objective function and a cost associated with maintaining the selected subtypes distinct." Because Karniewicz does not teach any of these limitations, it cannot be said to anticipate the invention as recited in claim 1. In addition, it cannot be said to anticipate or obviate any claims dependent on claim 1 for at least the reasons discussed. The Applicants invite the Examiner to identify portions of any of the cited references which teach these aspects of the claimed invention.

On page 10 of the office action, the Examiner attempted to correlate claim limitations with the various elements shown and described in Karniewicz with reference to Fig. 1(a). For example, the Examiner referred to the cell types 1, 2 and 3 on the different levels of the hierarchy shown in Fig. 1(a) as corresponding to the types and subtypes recited in the claims. The Applicants respectfully disagree with the Examiner's characterization of the reference.

As described in paragraphs [0026]-[0028] of Karniewicz, each cell type is the same as other cells of that type on the same level of the hierarchy. However, the cell types having the same numbers on different levels of the hierarchy are not related by type or subtype. Rather, a cell type on one level of the hierarchy is composed of some combination of cell types in the immediately lower level of the hierarchy. Cell types on one level of the hierarchy are not subtypes of cell types on another level of the hierarchy. As is well know and as described in the present specification, "'[s]ubtypes' of a particular cell type are schematically similar, but have differently sized transistors." See page 23, line 11. By contrast, Karniewicz's cell types on different levels of the hierarchy cannot be schematically similar in that they correspond to different levels of the overall system.

For example, higher order cell 100 is defined as relating 4 instances of basic atom cells 102, 104, 106 and 108 which correspond to atom cell types 1, 2, 3 and 1, respectively. However, it is clear from the context that atom cell type 1 (e.g., cell 102) is not the same as higher level cell type 1 (i.e., cell 100) and is certainly not a "subtype" which corresponds "to a particular cell type" and differs "from all other cell subtypes corresponding to the particular cell type by at least one transistor dimension" as recited in claim 1. Karniewicz confusingly reuses the cell type numbers on different levels of the hierarchy, but the numbers on different levels of the hierarchy obviously cannot refer to cells of the same type. Otherwise, the cell definitions, e.g., higher level cell 100, would have no meaning, i.e., they would be self-referential.

Thus, the Examiner's reference to paragraph [0035] as showing that "each cell type is divided into a plurality of subtypes" is incorrect. The "subtypes to which the Examiner refers are not subtypes at all, but different types of cells on a different level of the hierarchy. Paragraph [0035] merely describes how parameter changes made to the cells at the highest level of the hierarchy propagate downward through the device, higher order, and basic atom levels of the hierarchy.

Moreover, paragraph [0029] does not show "merging selected ones of the subtypes" resulting in fewer subtypes as claimed in claim 1. The language to which the Examiner refers merely describes how two different types of basic atom cells 102 and 104 may be combined to create a higher order cells 100 which might be, for example, a transistor. The paragraph goes on to describe that the parameters of the basic atom cells may be inherited by the higher order cell. However, basic atom cells 102 and 104 are not "subtypes" of cell 100. That is, they are not schematically similar. Rather, as described above, the cell type of cell 100 is merely defined as including these instances of different atom cell types. In addition, the combination of basic atom cells 102 and 104 does not result in fewer of anything. Rather, it results in an increase in the number of types of higher order cell types.

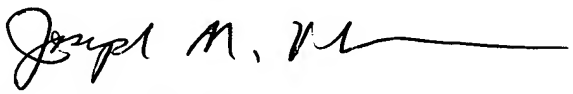
In view of the foregoing, the rejection of claim 1 over Karniewicz is believed overcome. In addition, the rejections of any claims depending on claim 1 are believed overcome for at least the reasons discussed.

The Examiner rejected claims 7, 8, 10, 12, 16 and 24 under 35 U.S.C. 103(a) as being unpatentable over Karniewicz in view of U.S. Patent No. 6,445,065 (Gheewala). The Examiner also rejected claims 29 and 31 under 35 U.S.C. 103(a) as being unpatentable over Karniewicz in view of U.S. Patent No. 5,790,415 (Pullela). In view of the foregoing discussion regarding claim 1, the rejections are believed overcome for at least the reasons discussed.

The Examiner objected to claims 13, 16, 24, 25 and 26 as being dependent on rejected base claims, but indicated the claims would be allowable if rewritten in independent form. The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter. However, in view of the foregoing discussion regarding claim 1, the Applicants believe the claims to which the Examiner objects are allowable in their current form.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 843-6200.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Joseph M. Villeneuve
Reg. No. 37,460

P.O. Box 778
Berkeley, CA 94704-0778
(510) 843-6200

map every unique instances into an instance class except for those cells in arrays. Once the cell instances are partitioned into instance classes, the circuit, i.e., each of the cell instances, is sized (804) using any of a variety of sizing tools such as, for example, the sizing tool described above. Because each of the cell instances is sized in this step without regard to the cost of introducing additional cell subtypes, a large number of cell subtypes, i.e., cells of a given type with different transistor sizes, will typically result. As mentioned above, the technique by which the circuit is sized is not particularly relevant to the most fundamental aspects of the invention, and may correspond to any of a wide variety of commercially available and proprietary integrated physical synthesis technologies.

As alluded to above, the designer is constrained by layout and verification resource in the number of subtypes which can be created and be part of the ultimate design. On the other hand, a sufficient number of cell subtypes is desirable to achieve a reasonable level of specialization in transistor sizes. Therefore, according to a specific embodiment of the invention, the various cell subtypes resulting from the sizing of 804 are grouped or merged with reference to a "profit function" (which provides a measure of the benefit to be gained by a particular grouping) to form a smaller set of subtypes (806).

A profit function for use with the present invention may take into account a variety of metrics such as, for example, chip area savings and/or the layout cost associated with the number of subtypes. Different embodiments may consider any or all such metrics, as well as approximations thereof. For example, chip area savings may be determined by performing a test sizing for each grouping decision. Alternatively, to save time, more easily derived rough estimates may be employed. In some exemplary embodiments, layout cost may be ignored. According to others, a rough estimate may be employed.

According to various specific embodiments, a variety of grouping techniques may be employed. According to one such embodiment, potential groupings are determined by

Docket #	FULCP004X1	By:	JMV/th	Date of this mailing:	July 14, 2003
Appl'n # :	Not yet assigned	Filing Date:	July 14, 2003	Express Mail #	EV332825444US
Inv(s)	Frederik Eaton and Peter Beerel				
Title:	OPTIMIZATION OF CELL SUBTYPES IN A HIERARCHICAL DESIGN FLOW				

21909 U S PTO
10/620330
07/14/03

The following have been received in the U.S. Patent Office on the date stamped hereon:

Item	*Description*	*# Pgs*
1.	Utility Patent Application Transmittal w/ certificate of Express Mailing	03
2.	Specification, Claims, and Abstract	45
3.	Formal Drawings	08
4.		
5.		
6.		

BEYER WEAVER & THOMAS LLP
Docketed Date
JUL 25 2003
BERKELEY CA
JMV/JMV